## <u>CLAIMS</u>

What is claimed is:

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1 1.\ An integrated circuit comprising:

a performance circuit occupying a first area of an

integrated circuit substrate; and

4 a protection circuit coupled to the performance circuit

5 and having a size commensurate with dissipating an amount of

predetermined charge incident on the performance circuit and

occupying a second area of an integrated circuit substrate

separate from the first area.

- 2. The integrated circuit of claim 1, wherein the performance circuit is configured to one of accept and drive a signal external to the/integrated circuit.
- 3. The integrated circuit of claim 1, wherein the protection circuit is a diode.
- 1 4. The integrated circuit of claim 1, wherein the
- 2 protection circuit includes:
- a diode comprised of a unit block of a doped region of
- 4 the integrated circuit substrate occupying an area of the
- 5 substrate sufficient to support a contact to the doped region;
- a junction region of the integrated circuit substrate

7 surrounding the doped region; and

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a contact to the doped region.

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- 1 5. The integrated circuit of claim 4, the doped region
- 2 being a first doped region of a first dopant in a well of the
- 3 substrate, the well being doped with a first concentration of a
- 4 second dopant and the junction region separating the first doped
- 5 region from the well, the diode comprising a third doped region in
- 6 the well adjacent the junction region, the third doped region
- 7 doped with a second concentration of the second dopant.
  - 6. The integrated circuit of claim 5, wherein the diode is comprised of a plurality of unit blocks, each of the plurality of unit blocks having a first doped region of a first dopant in a well of the substrate and a junction region separating each of the first doped regions from the well.
  - 7. The integrated circuit of claim 6, wherein the third doped region surrounds the junction.
- 1 8. The integrated circuit of claim 1, wherein the
- 2 performance circuit includes:
- a unit transistor having a drain region comprised of a
- 4 unit block of a doped region of the integrated circuit substrate
- 5 occupying an area of the substrate sufficient to support a contact
- 6 to the doped region;
- 7 a gate region of the integrated circuit substrate
- 8 surrounding the drain region; and

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- 9 a contact to the doped region.
- 1 9. The integrated circuit of claim 8, the doped region
- 2 having a first dopant in a well of the substrate, the well being
- 3 doped with a second dopant, the transistor comprising a source
- 4 region having the first dopant in the well separated from the
- 5 drain region by the gate.
- 1 10. The integrated circuit of claim 9, wherein the
- 2 performance circuit includes a plurality of unit transistors.
  - 11. A buffer comprising:

complimentary metal oxide semiconductor (CMOS) device occupying a first area of an integrated circuit substrate; and

a protection circuit including a diode coupled to the CMOS device and occupying a second area of an integrated circuit substrate separate from the first area, the diode having a size commensurate with dissipating an amount of predetermined charge incident on the performance circuit.

- 1 12. The buffer of claim 11, wherein the buffer is one of an
- 2 input buffer, an output buffer, and an input/output buffer.
- 1 13. The buffer of claim 11, wherein the CMOS device includes
- 2 a p-channel device and the diode is coupled to the p-channel
- 3 device.

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- 1 14. The buffer of claim 13, the diode including:
- a diode comprised of a plurality of unit blocks, each of
- 3 the plurality of unit blocks having a p-doped region in an n-well
- 4 of the substrate\and occupying an area of the substrate sufficient
- 5 to support a contact to the p-doped region;
- a junction region separating each of the p-doped regions
- 7 from the n-well; and
- a contact to each of the plurality of unit blocks.
  - 15. The buffer of claim 14, the diode further comprising an n-doped region adjacent the junction of each p-doped region, the n-doped region doped with a dopant concentration greater than a dopant concentration of the n-well.
  - 16. The buffer of claim 15, wherein the n-doped region surrounds the junction.
  - 17. The buffer of claim 11, wherein the CMOS device
- 2 comprises:

- a unit transistor having a drain region comprised of a
- 4 unit block of a p-doped region in a well of the integrated circuit
- 5 substrate, the unit block occupying \an area of the substrate
- 6 sufficient to support a contact to the p-doped region;
- 7 a gate region of the integrated circuit substrate
- 8 surrounding the p-doped region; and
- a contact to the p-doped region.

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- 1 18. The buffer of claim 17, the well being doped with a
- 2 first concentration of an n-type dopant, the unit transistor
- 3 comprising a p-doped source region in the well separated from the
- 4 drain region by the gare
- 1 19. The buffer of claim 18, wherein the complimentary metal
- 2 oxide semiconductor device comprises a plurality of unit
- 3 transistors.

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A method of forming an integrated circuit comprising:

forming a performance circuit occupying a first area of
an integrated circuit substrate;

forming a protection circuit occupying a second area of an integrated circuit substrate separate from the first area; and coupling the protection circuit to the performance circuit.

- 21. The method of claim 20, wherein the step of forming a performance circuit includes a forming a CMOS device.
  - 22. The method of claim 21, wherein the step of coupling the protection circuit to the performance circuit includes coupling the protection circuit to a p-channel device of the CMOS device.
- 1 23. The method of claim 21, wherein the step of forming a
- 2 protection circuit includes forming a diode and the step of

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- 3 coupling the protection circuit to the performance circuit
- 4 includes coupling the diode to the p-channel device  $\phi$ f the CMOS.
- 1 24. The method of claim 20, wherein the step of forming a
- 2 protection circuit includes forming a unit diode, the unit diode
- 3 comprised of a block of a doped region of the integrated circuit
- 4 substrate occupying an area of the substrate sufficient to support
- 5 a contact to the doped region, a junction fegion of the integrated
- 6 circuit substrate surrounding the doped region, and a contact to
- 7 the doped region.

- 25. The method of claim 20, the doped region being a first doped region of a first dopant in a well of the substrate, the well being doped with a first concentration of a second dopant and the junction region separating the first doped region from the well, wherein the step of forming a protection circuit includes forming a third doped region in the well adjacent the junction region, the third doped region doped with a second concentration of the second dopant.
- 1 26. The method of claim 25, wherein the step of forming a
- 2 protection circuit includes forming a plurality of unit diodes.
- 1 27. The method of claim 20, wherein the step of forming a
- 2 performance circuit includes:
- forming a unit transistor device having a drain region
- 4 comprised of a doped region of the integrated circuit substrate

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occupying an area sufficient to support a contact to the doped region;

forming a gate region of the integrated circuit substrate surrounding the doped region; and forming a contact to the doped region.

The method of claim 27, the doped region being a first doped region of a first dopant in a well of the substrate, the well being doped with a concentration of a second dopant and the step of forming a performance circuit further comprises:

forming a source region of the transistor doped with the first dopant in the well separated from the drain region by the gate to form a unit transistor.

29. The method of claim 28, wherein the step of forming a performance circuit includes:

forming a plurality of unit transistors.

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